AMENDMENT TO THE SPECIFICATION

Please replace the paragraph beginning on line 1 of page 20 with the following paragraph:

Referring now to step 740 of Figure 7, when the number of stages (e.g., delay elements 610 and 611 of Figure 6) is known, the delay chain is configured in a closed loop mode as a VCO. In embodiments of the present invention, when phase detector 420 determines that a sufficient match between the phases of the two signals or a "coarse lock," has been achieved, it then generates a second signal via fine_en signal path 422 for dynamically switching circuit 430 from a delay lock loop mode to a phased locked loop, or " "closed loop," mode. In embodiments of the present invention, this signal determines which signal path either vcdl_in 401 or vco_in_out, will be the input for delay block 510a. This signal also couples/decouples multiplexor 530b with the signal path for phase generator 430. After switching to a phase locked loop mode, the input signal received via vcdl_in signal path 401 is disengaged and the vco_in_out signal path 550 [[560]] is now the input to delay block 520a. In this mode, the delay stages associated with circuits 510c and 510d are bypassed.

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